L	Hits	Search Text	DB	Time stamp
Number	0157	(atmoss adi2 tost(2) on (burn-in adi2	HCDATT.	2004/01/15
1	9157	(stress adj2 test\$3) or (burn-in adj2 test\$3)	USPAT; EPO; JPO; DERWENT	2004/01/15 11:23
2	1019	((stress adj2 test\$3) or (burn-in adj2 test\$3)) near5 (IC or (integrated adj2	USPAT; EPO; JPO;	2004/01/15 10:03
3	1154	<pre>circuit\$1))  ((stress adj2 test\$3) or (burn-in adj2 test\$3)) near10 (IC or (integrated adj2</pre>	DERWENT USPAT; EPO; JPO;	2004/01/15 10:03
4	830	circuit\$1))	DERWENT USPAT; EPO; JPO;	2004/01/15
5	149	circuit\$1)) (((stress adj2 test\$3) or (burn-in adj2	DERWENT USPAT;	2004/01/15
6	418	<pre>test\$3)) near3 (IC or (integrated adj2 circuit\$1))) and (latch\$2 or flip-flop\$1) (((stress adj2 test\$3) or (burn-in adj2</pre>	EPO; JPO; DERWENT USPAT;	2004/01/15
		test\$3)) near3 (IC or (integrated adj2 circuit\$1))) and (plurality or multiple near3 (latch\$2 or flip-flop\$1))	EPO; JPO; DERWENT	10:25
7	12		USPAT; EPO; JPO; DERWENT	2004/01/15 10:29
8	121	(stress\$3 near3 (IC or (integrated adj2 circuit\$1))) and (latch\$2 or flip-flop\$1)	USPAT; EPO; JPO;	2004/01/15 10:32
9	83	(stress\$3 adj3 (IC or (integrated adj2 circuit\$1))) and (latch\$2 or flip-flop\$1)	DERWENT USPAT; EPO; JPO; DERWENT	2004/01/15
10	15	<pre>(stress\$3 adj3 (IC or (integrated adj2 circuit\$1))) same (latch\$2 or flip-flop\$1)</pre>	USPAT; EPO; JPO; DERWENT	2004/01/15
11	15		USPAT; EPO; JPO; DERWENT	2004/01/15 10:33
12	0		USPAT; · EPO; JPO;	2004/01/15 10:36
13	0	circuit\$1))) and ((scan adj2 design\$1) or	DERWENT USPAT; EPO; JPO;	2004/01/15 10:36
16	0	LSSD) (stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) and (714/726.ccls.)	DERWENT USPAT; EPO; JPO;	2004/01/15 10:38
17	o	   (stress\$3 adj3 (IC\$1 or (integrated adj2  circuit\$1))) and (714/727.ccls.)	DERWENT USPAT; EPO; JPO;	2004/01/15 10:38
14	3	(stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) and ((scan adj2 test\$3) or	DERWENT USPAT; EPO; JPO;	2004/01/15 10:38
15	5	LSSD) (stress\$3 adj3 (IC\$1 or (integrated adj2  circuit\$1))) and (714/724.ccls.)	DERWENT USPAT; EPO; JPO;	2004/01/15 11:06
18	0	(stress\$3 adj3 (IC\$1 or (integrated adj2 circuit\$1))) and (714/!.ccls.)	DERWENT USPAT; EPO; JPO;	2004/01/15 11:07
19	21	((stress adj2 test\$3) or (burn-in adj2 test\$3)) and LSSD	DERWENT USPAT; EPO; JPO;	2004/01/15 13:12
20	972	(reduc\$4 near5 current) near10 test\$3	DERWENT USPAT; EPO; JPO;	2004/01/15 13:13
21	20	(reduc\$4 near5 current) near10 ((stress or burn-in) adj4 test\$3)	DERWENT USPAT; EPO; JPO;	2004/01/15 13:14
22	52		DERWENT USPAT; EPO; JPO;	2004/01/15 13:26
			DERWENT	

Search History 1/15/04 3:53:49 PM Page 1

100

23	1279	test\$3) near10 ((integrated adj2 circuit)	USPAT; EPO; JPO;	2004/01/15 13:28
24	956	or IC\$2) ((stress or burn-in or accelerat\$4) adj2 test\$3) near4 ((integrated adj2 circuit)	DERWENT USPAT; EPO; JPO;	2004/01/15 13:50
25	869	or IC\$2)	DERWENT USPAT;	2004/01/15
		((integrated adj2 circuit) or IC\$2)	EPO; JPO; DERWENT	13:50
26	1	<pre>(((stress or burn-in) adj2 test\$3) near4 ((integrated adj2 circuit) or IC\$2)) same (reduc\$5 near3 current)</pre>	USPAT; EPO; JPO; DERWENT	2004/01/15 13:51
27	27	(((stress or burn-in) adj2 test\$3) near4 ((integrated adj2 circuit) or IC\$2)) and	USPAT; EPO; JPO;	2004/01/15 13:58
28	4	<pre>(reduc\$5 near3 current) ((stress adj2 test\$3) near4 ((integrated adj2 circuit) or IC\$2)) and (reduc\$5</pre>	DERWENT USPAT; EPO; JPO;	2004/01/15 14:00
29	35	near3 current) (test\$3 near2 ((integrated adj1 circuit) or IC\$2)) same (reduc\$5 near3 current)	DERWENT USPAT; EPO; JPO;	2004/01/15 14:01
30	421	(test\$3 near2 ((integrated adj1 circuit) or IC\$2)) and (reduc\$5 near3 current)	DERWENT USPAT; EPO; JPO; DERWENT	2004/01/15 14:01
31	75	<pre>(test\$3 near2 ((integrated adj1 circuit) or IC\$2)) and (reduc\$5 near3 current) and flip-flop\$1</pre>	USPAT; EPO; JPO; DERWENT	2004/01/15 14:02
32	163		USPAT; EPO; JPO; DERWENT	2004/01/15 14:02
33	23	(test\$3 near2 ((integrated adj1 circuit) or IC\$2)) and (reduc\$5 near3 current) and ((plurality or multiple) adj3	USPAT; EPO; JPO; DERWENT	2004/01/15 14:03
34	58	(flip-flop\$1 or latch\$3)) (test\$3 near2 (circuit or IC\$2)) and (reduc\$5 near3 current) and ((plurality or multiple) adj3 (flip-flop\$1 or	USPAT; EPO; JPO; DERWENT	2004/01/15 14:26
35	7	latch\$3)) (test\$3 adj2 IC\$2) and (reduc\$5 near3 current) and ((plurality or multiple)	USPAT; EPO; JPO;	2004/01/15 14:26
36	8	adj3 (flip-flop\$1 or latch\$3)) (test\$3 near2 IC\$2) and (reduc\$5 near3 current) and ((plurality or multiple)	DERWENT USPAT; EPO; JPO;	2004/01/15 14:33
37	105	<pre>adj3 (flip-flop\$1 or latch\$3)) bernstein-k\$.in.</pre>	DERWENT USPAT; EPO; JPO;	2004/01/15 14:37
39	13	bernstein-k\$.in.and test\$3	DERWENT USPAT; EPO; JPO;	2004/01/15 14:38
38	3	bernstein-k\$.in.and stress\$3	DERWENT USPAT; EPO; JPO;	2004/01/15 14:54
40	3	VDD0 and VDD1 and VDD2	DERWENT USPAT; EPO; JPO; DERWENT	2004/01/15 15:00
41	14930	(first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))	USPAT; EPO; JPO; DERWENT	2004/01/15 15:01
42	1730	((first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))) and ((first adj2 logic) or (second adj3 logic))	USPAT; EPO; JPO; DERWENT	2004/01/15 15:03
43	504	((first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))) same ((first adj2 logic) or (second adj3	USPAT; EPO; JPO; DERWENT	2004/01/15 15:03
44	133	<pre>logic)) (((first adj3 (latch or flip-flop)) same (second adj3 (latch or flip-flop))) same ((first adj2 logic) or (second adj3 logic))) and test\$3</pre>	USPAT; EPO; JPO; DERWENT	2004/01/15 15:03
	<u> </u>	Togic/// and tests	<u> </u>	L

Search History 1/15/04 3:53:49 PM Page 2

45	10	(((first adj3 (latch or flip-flop))	same	USPAT;	2004/01/15
		(second adj3 (latch or flip-flop)))	same	EPO; JPO;	15:49
		((first adj2 logic) or (second adj3		DERWENT	
:		logic))) and test\$3 and LSSD		<i>A</i> .	
46	26	(((first adj3 (latch or flip-flop))	same	USPAT;	2004/01/15
		(second adj3 (latch or flip-flop)))	same	EPO; JPO;	15:04
		((first adj2 logic) or (second adj3		DERWENT	
		logic))) and (scan adj2 test\$3)			
47	12	(((first adj3 (latch or flip-flop))	same	USPAT;	2004/01/15
		(second adj3 (latch or flip-flop)))	same	EPO; JPO;	15:50
		((first adj2 logic) or (second adj3		DERWENT	
1		logic))) and LSSD			